11-08-00 A

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P1674D4

First Named Inventor or Application Identifier Jack D. Pippin

Express Mail Label No. EL609099511US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 34)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 11)

4. X Oath or Declaration/Power of Attorney (Total Pages 5)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. ____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ___ Computer Readable Copy
b. ___ Paper Copy (identical to computer copy)
c. ___ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _X_ Assignment Papers (cover sheet & documents(s))

9. ____ 37 CFR 3.73(b) Statement (where there is an assignee)

10. ____ English Translation Document (if applicable)

11. _X_ a. Information Disclosure Statement (IDS)/PTO-1449

_X_ b. Copies of IDS Citations

12. ____ Preliminary Amendment

13. _X_ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. ____ a. Small Entity Statement(s)

____ b. Statement filed in prior application, Status still proper and desired

15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. ____ Other: _____

_____

_____

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17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation _X_ Divisional ____ Continuation-in-part (CIP)

of prior application No: 08/660,016

18. **Correspondence Address**

____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)

or

_X_ Correspondence Address Below

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FEE TRANSMITTAL FOR FY 2001

TOTAL AMOUNT OF PAYMENT ($) $750.00

Complete if Known:
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Filing Date Concurrently Herewith
First Named Inventor Jack D. Pippin
Group Art Unit Not yet assigned
Examiner Name Not yet assigned
Attorney Docket No. 042390.P1674D4

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility application filing fee	710.00
106	320	206	160	Design application filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 710.00

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	19	– 20** =	0	X 18.00 =	
Independent Claims	2	– 3** =	0	X 80.00 =	
Multiple Dependent				=	

**Or number previously paid, if greater; For Reissues, see below.

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 0.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	390	216	195	Extension for response within second month	
117	890	217	445	Extension for response within third month	
118	1,390	218	695	Extension for response within fourth month	
128	1,890	228	945	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,240	241	620	Petition to revive unintentionally abandoned application	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	710	246	355	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	710	249	355	For each additional invention to be examined (see 37 CFR 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

Other fee (specify) _____

SUBTOTAL (3) $ 40.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

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Reg. Number: 33,192 Telephone Number: 303-740-1980 ext. 211

Docket No. 042390.P1674D4 Patent Application

UNITED STATES PATENT APPLICATION

FOR

FAIL-SAFE THERMAL SENSOR APPARATUS AND METHOD

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April M. Worley
Name of Person Mailing Correspondence

April M. Worley
Signature

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Date

FAIL-SAFE THERMAL SENSOR APPARATUS AND METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a division of prior application Serial No. 09/093,988 filed June 8, 1998 which is a continuation of prior application Serial No. 08/660,016, filed June 6, 1996, issued as U.S. Patent No. 5,838,578 on November 17, 1998, which is a continuation of prior application Serial No. 08/124,980, filed September 21, 1993, all entitled "Method and Apparatus for Programmable Thermal Sensor for an Integrated Circuit" and all assigned to the assignee of the present application.

FIELD OF THE INVENTION

The present invention relates to thermal sensing, and more specifically to methods and apparatus for a programmable thermal sensor in an integrated circuit.

ART BACKGROUND

Advances in silicon process technology has lead to the development of increasingly larger die sizes for integrated circuits. The large dies sizes permit integration of millions of transistors on a single die. As die sizes for integrated circuits become larger, the integrated circuits consume more power. In addition, advances in microprocessor computing require execution of a large number of instructions per second. To execute more instructions per second, the microprocessor circuits operate at an increased clock frequency. Therefore, a microprocessor containing over one million transistors may consume over 30 watts of power. With large amounts of power being dissipated, cooling becomes a problem.

Typically, integrated circuits and printed circuit boards are cooled by either active or passive cooling devices. A passive cooling device, such as a heat sink mounted onto an integrated circuit, has a limited capacity to dissipate heat. An active cooling device, such as a fan, is used to dissipate larger amounts of heat. Although a fan cooling system dissipates heat, there are several disadvantages associated with such a system. Traditionally, fans cool integrated circuits by air convection circulated by a fan. However, when a fan is used in conjunction with a high density multi-chip computer system, a large volume of air is required for cooling thereby necessitating powerful blowers and large ducts. The powerful blowers and large ducts implemented in the computer occupy precious space and are too noisy. The removal of a cover or other casing may result in a disturbance of air flow causing the fan cooling system to fail. In addition, the fan cooling system is made up of mechanical parts that have a mean time between failure (MTBF) specification less than a typical integrated circuit. Furthermore, fan cooling systems introduce noise and vibration into the system.

In addition to cooling systems, thermal sensors are implemented to track the temperature of an integrated circuit or electronic system. Typically, thermal sensors consist of a thermocouple which is directly attached to a heat sink. In more sophisticated thermal sensing systems, a diode and external analog circuitry are used. In operation, the voltage/current characteristics of the diode change depending upon the temperature of the integrated circuit, and the external analog circuitry measures the voltage or current characteristics of the diode. The additional analog circuitry is complex and difficult to implement. In addition, employing the analog circuitry results in a thermal time delay degrading the accuracy of such a configuration. Moreover, external analog circuitry for

sensing the voltage of the diode consumes a larger area than the integrated circuit being sensed. Therefore, it is desirable to provide a thermal sensor which is incorporated into the integrated circuit. In addition, it is desirable to provide a thermal sensor that can provide feedback for an active cooling system. Furthermore, it is desirable to control the temperature of an integrated circuit without the use of a fan. The present invention provides an integrated thermal sensor that detects a threshold temperature so that active cooling of the integrated circuit is accomplished through system control.

SUMMARY OF THE INVENTION

A programmable thermal sensor is implemented in an integrated circuit. The programmable thermal sensor monitors the temperature of the integrated circuit, and generates an output to indicate that the temperature of the integrated circuit has attained a predetermined threshold temperature. The programmable thermal sensor contains a voltage reference, a programmable V_{be}, a current source, and a sense amplifier or comparator. The current source generates a constant current to power the voltage reference and the programmable V_{be}. With a constant current source, the voltage reference generates a constant voltage over varying temperatures and power supply voltages. In a preferred embodiment, the voltage reference is generated with a silicon bandgap reference circuit. The constant voltage from the voltage reference is one input to the sense amplifier. The programmable V_{be} contains a sensing portion and a multiplier portion. In general, the programmable V_{be} generates a voltage dependent upon the temperature of the integrated circuit and the value of programmable inputs. The programmable inputs are supplied to the multiplier portion to generate a multiplier value for use in the multiplier portion. The voltage reference is compared with the voltage generated by the programmable V_{be} in the sense amplifier. The sense amplifier generates a greater than, less than, signal.

The programmable thermal sensor of the present invention is implemented in a microprocessor. In addition to the programmable thermal sensor, the microprocessor contains a processor unit, an internal register, microprogram and clock circuitry. The processor unit incorporates the functionality of any microprocessor circuit. The clock circuitry generates a system clock for operation of the microprocessor. In general, the

microprogram writes programmable input values to the internal register. The programmable input values correspond to threshold temperatures. The programmable thermal sensor reads the programmable input values, and generates an interrupt when the temperature of the microprocessor reaches the threshold temperature. In a first embodiment, the interrupt is input to the microprogram and the processor unit. In response to an interrupt, the processor unit may take steps to cool the temperature of the microprocessor, and the microprogram programs a new threshold temperature. For example, the processor may turn on a fan or reduce the clock frequency. The new threshold temperature is slightly higher than the current threshold temperature so that the processor unit may further monitor the temperature of the microprocessor.

In a second embodiment of the present invention, the interrupt generated by the programmable thermal sensor is input to external sensor logic. The external sensor logic automatically controls the frequency of the microprocessor. If the temperature of the microprocessor raises, then the clock frequency is decreased. Conversely, if the temperature of the microprocessor drops, then the system clock frequency is increased. In addition to a programmable thermal sensor, the microprocessor contains a fail safe thermal sensor. The fail safe thermal sensor generates an interrupt when detecting that the microprocessor reaches pre-determined threshold temperatures and subsequently halts operation of the system clock. The predetermined threshold temperature is selected below a temperature that causes physical damage to the device. The microprocessor of the present invention is implemented in a computer system. Upon generation of an interrupt in the programmable thermal sensor, a message containing thermal sensing information is generated and displayed to a user of the computer system.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features, and advantages of the present invention will be apparent from the following detailed description of the preferred embodiment of the invention with references to the following drawings.

FIG. 1 illustrates a block diagram of a programmable thermal sensor configured in accordance with the present invention.

FIG. 2 illustrates a graph depicting the relationship between the base-emitter voltage (V_{be}) of a bipolar transistor versus the temperature of the supply voltage.

FIG. 3 illustrates a bandgap reference circuit configured in accordance with the present invention.

FIG. 4 illustrates a programmable base to emitter voltage (V_{be}) circuit configured in accordance with the present invention.

FIG. 5 illustrates a current source, including the bandgap reference circuit, configured in accordance with the present invention.

FIG. 6 illustrates a sense amplifier for the thermal sensor configured in accordance with the present invention.

FIG. 7 illustrates block diagram of a first embodiment of a microprocessor incorporating a programmable thermal sensor configured in accordance with the present invention.

FIG. 8 illustrates a flow diagram for a method of controlling the programmable thermal sensor configured in accordance with the present invention.

FIG. 9 illustrates a block diagram of a second embodiment of a microprocessor incorporating a programmable thermal sensor configured in accordance with the present invention.

FIG. 10 illustrates a block diagram of a microprocessor incorporating a fail safe thermal sensor configured in accordance with the present invention.

FIG. 11 illustrates a computer system incorporating a microprocessor comprising thermal sensing configured in accordance with the present invention.

NOTION AND NOMENCLATURE

The detailed descriptions which follow are presented, in part, in terms of algorithms and symbolic representations of operations within a computer system. These algorithmic descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art.

An algorithm is here, and generally, conceived to be a self-consistent sequence of steps leading to a desired result. These steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It proves convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Further, the manipulations performed are often referred to in terms, such as adding or comparing, which are commonly associated with mental operations performed by a human operator. No such capability of a human operator is necessary, or desirable in most cases, in any of the operations described herein which form part of the present invention; the operations are machine operations. Useful machines for performing the operations of the present invention include general purpose digital computers or other similar devices. In all cases there should be borne in mind the distinction between the method operations in operating a computer and the method of computation itself. The

present invention relates to method steps for operating a computer in processing electrical or other (e.g., mechanical, chemical) physical signals to generate other desired physical signals.

The present invention also relates to apparatus for performing these operations. This apparatus may be specially constructed for the required purposes or it may comprise a general purpose computer as selectively activated or reconfigured by a computer program stored in the computer. The algorithms presented herein are not inherently related to a particular computer or other apparatus. In particular, various general purpose machines may be used with programs written in accordance with the teachings herein, or it may prove more convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these machines will appear from the description given below. Machines which may perform the functions of the present invention include those manufactured by Intel Corporation, as well as other manufacturers of computer systems.

DETAILED DESCRIPTION

Methods and apparatus for thermal sensing in an integrated circuit are disclosed. In the following description, for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required to practice the present invention. In other instances, well known circuits and devices are shown in block diagram form to avoid obscuring the present invention unnecessarily.

Referring to FIG. 1, a block diagram of a programmable thermal sensor configured in accordance with the present invention is illustrated. In general, a programmable thermal sensor 100 monitors the temperature of an integrated circuit, and generates an output to indicate that the temperature of the integrated circuit has attained a predetermined threshold temperature. The programmable thermal sensor 100 contains a voltage reference 120, a programmable V_{be} 110, a current source 140, and a sense amplifier 160. The current source 140 generates a constant current to power the voltage reference 120 and the programmable V_{be} 110. With a constant current source, the voltage reference 120 generates a constant voltage over varying temperatures and power supply voltages (Vcc). In a preferred embodiment, the voltage reference is generated with a silicon bandgap reference circuit. The constant voltage from the voltage reference 120 is input to the sense amplifier 160. The programmable V_{be} 110 contains a sensing portion and a multiplier portion. In general, the programmable V_{be} 110 generates a voltage dependent upon the temperature of the integrated circuit and the value of programmable inputs. The programmable inputs are supplied to the multiplier portion to generate a multiplier value for use in the multiplier portion.

Referring to FIG. 2, a graph depicting the relationship between the base-emitter voltage (V_{be}) of a bipolar transistor versus temperature is illustrated. A characteristic curve 200 on the graph of FIG. 2 shows the linear characteristics of the V_{be} voltage over a temperature range of 70 degrees Fahrenheit (70° F.) to 140° F. In addition, the graph of FIG. 2 shows a relative constant bandgap voltage curve 205 over the specified temperature range. Although the bandgap voltage varies slightly over the temperature range, the variation of the bandgap voltage is negligible compared to the variation of the V_{be} voltage over the temperature range. As shown by the curve 205 in FIG. 2, the bandgap voltage is equal to approximately 1.3 volts (V). When the V_{be} voltage equals 1.3 volts, the temperature of the integrated circuit is 100° F. Based on the linear temperature characteristics of the V_{be} voltage, and the relatively constant bandgap voltage over the temperature range, a thermal sensor is constructed.

For the voltage/temperature characteristics of line 200 shown in FIG. 2, the bandgap voltage equals the V_{be} voltage when the integrated circuit is at 100° F. However, the V_{be} voltage may be changed to sense additional temperature values in the integrated circuit. By shifting the linear V_{be} voltage/temperature characteristic curve 200, any number of predetermined threshold temperature values are detected. To shift the voltage/temperature characteristic curve 200, the V_{be} voltage is multiplied by pre-determined values to generate a new voltage for comparison to the bandgap voltage. Specifically, to shift the characteristic curve 200 to sense a voltage less then 100° F., the V_{be} voltage is multiplied by a fraction to generate a new characteristic curve, such as the characteristic curve 210 shown in FIG. 2. The characteristic curve 210 exhibits the same slope as the original characteristic curve 200. However, for the characteristic curve 210,

the V_{be} voltage is equal to the bandgap voltage when the integrated circuit temperature equals 90° F. Similarly, the V_{be} voltage may be multiplied by a value greater than 1 to generate a characteristic curve such as the characteristic curve 220 shown in FIG. 2. The characteristic curve 220 also exhibits the same slope as the original characteristic curve 200. However, the characteristic curve 220 intersects the bandgap voltage curve 205 at 120°F. Consequently, any number of threshold temperatures are detectable by multiplying the V_{be} voltage by a predetermined constant.

Referring to FIG. 3, a bandgap reference circuit configured in accordance with the present invention is illustrated. The bandgap reference circuit 120 is powered from a voltage source, Vcc. The voltage source Vcc is regulated by a current source such that the current source 140 supplies a constant current over a wide range of Vcc voltages. A preferred embodiment of the present invention for the current source 140 is described fully below. The bandgap reference circuit 120 contains three N-P-N bipolar transistors Q1, Q2 and Q3, and three resistive elements R1, R2 and R3. In general, the constant bandgap reference voltage, $V_{bandgap}$, is generated at the collector of N-P-N transistor Q3. The bipolar transistors Q1, Q2 and resistive elements R1, R2 and R3 are provided to compensate for temperature variations in the base to emitter junction voltage (V_{be}) of bipolar transistor Q3. Specifically, the resistive element R1 is coupled from the current source 140 to the collector of bipolar transistor Q1. The collector and base of bipolar transistor Q1 are shorted so that Q1 is effectively a P-N junction diode. The base of transistor Q1 and the base of transistor Q2 are coupled together. The resistive element R3 couples the collector of transistor Q2 to the current source 140, and the resistive element R2 couples the emitter of transistor Q2 to ground. In a preferred embodiment of

the present invention, the resistive element R1 equals 4800 ohms, the resistive element R2 equals 560 ohms, and the resistive element R3 equals 4800 ohms.

In operation, the voltage at the base of transistors Q1 and Q2 are pulled to the $V_{bandgap}$ voltage through the R1 resistance. Therefore, the transistors Q1 and Q2 are biased in the active region, thereby allowing current to flow from the collector to the emitter of transistors Q1 and Q2. The mirrored configuration of transistors Q1 and Q2 tends to drive the base to emitter voltage (V_{be}) of transistors Q1 and Q2 equivalent. However, the resistive element R2 increases the resistance at the emitter of transistor Q2, resulting in a greater current density flowing through transistor Q1 than flowing through transistor Q2. As the temperature in the integrated circuit rises, the V_{be} of transistor Q2 decreases. In turn, the decrease of V_{be} on transistor Q2 causes a decrease in the current density flow through Q2. The decrease in current density through the resistive element R2 also causes a reduction in the current density flowing through the resistive element R3. Because the collector of transistor Q2 is coupled to the base of transistor Q3, a decrease in the current through resistive element R3 results in an increase in the voltage at the base of transistor Q3. Consequently, as the temperature of the integrated circuit rises, the V_{be} across transistors Q1, Q2, and Q3 decreases. However, the decrease of V_{be} on transistor Q3 is compensated by the increase of voltage at the base of transistor Q3. Therefore, regardless of temperature fluctuations, the $V_{bandgap}$ remains at a constant silicon bandgap voltage. For a further explanation of generation of a bandgap reference, including a theoretical derivation, see A. T. Brokaw, A Simple Three-Terminal IC Bandgap Reference, IEEE J. of Solid State Circuits, December, 1974, and Karel E. Kuijk, A Precision Reference Voltage Source, IEEE J. of Solid State Circuits, June 1973.

Referring to FIG. 4, a programmable base to emitter voltage (V_{be}) circuit configured in accordance with the present invention is illustrated. In a preferred embodiment of the present invention, a temperature varying voltage is generated from the characteristics of a base to emitter junction on a bipolar transistor. In general, the programmable V_{be} circuit generates an output voltage, V_{out}, based on the V_{be} voltage and the value of programmable input voltages V_{p1}, V_{p2} and V_{p3}. A N-P-N bipolar transistor Q11 shown in FIG. 4 is utilized to generate the V_{be} reference voltage. As described above, the V_{be} /temperature characteristic curve may be shifted along the temperature axis to detect a desired threshold temperature. By shifting the V_{be} /temperature characteristic curve along the temperature axis, a plurality of output voltages representing different threshold temperatures are generated.

To generate the V_{out} for a particular threshold temperature, a programmable V_{be} multiplier circuit is utilized. The programmable V_{be} multiplier circuit contains resistive elements R5, R6, R7, R8, and R9, and metal oxide semiconductor field effect transistors (MOSFET) Q12, Q13, and Q14. In a preferred embodiment, Q12, Q13 and Q14 comprise N-MOS transistors. The drain terminal of transistor Q12 is coupled to a first input on resistive element R7, and the source of transistor Q12 is coupled to a second input on resistive element R7. The transistors Q13 and Q14 are similarly coupled to resistive elements R8 and R9, respectively. Programmable input voltages V_{p1}, V_{p2}, and V_{p3} are input to the gate of transistors Q12, Q13 and Q14, respectively. The input voltages V_{p1}, V_{p2}, and V_{p3} control the current flow by selecting either a resistive element or the respective MOS transistor.

In operation, the programmable V_{be} multiplier circuit outputs a voltage, V_{out}, comprising a multiple of the base to emitter voltage on bipolar transistor Q11. For purposes of explanation, consider resistive elements R6, R7, R8 and R9 as one resistive element: R6-R9. The resistive element R6-R9 is connected across the base to emitter junction of bipolar transistor Q11. Therefore, the voltage drop across the resistive element R6-R9 is equivalent to V_{be} of bipolar transistor Q11. The current flowing through resistive element R6-R9 is approximately equal to the current flowing through resistive element R5 minus the current flowing into the base of transistor Q11. Therefore, if the value of resistive element R5 is equal to the value of resistive element R6-R9, the voltage at the collector of transistor Q11 equals $2V_{be}$. In general, the V_{out} voltage is defined by the following equation:

$V_{out} = V_{R5} + V_{be}$

$V_{be} = V_{R6\text{-}R9}$

$V_{out} = V_{R5} + V_{R6\text{-}R9}$

Therefore, V_{out} values greater than $1V_{be}$ are generated by changing the ratio between resistive element R5 and resistive element R6-R9.

To move the V_{be} curve 200 shown in FIG. 2 along the temperature axis via the programmable V_{be} circuit 110, a combination of resistive elements R7, R8 and R9 are selected. To select a combination of resistive elements R7, R8 and R9, the voltages Vp1, Vp2, and Vp3 are applied to the gates of MOS transistors Q13, Q12, and Q14, respectively. The resistive elements R7, R8 and R9 are binary weighed resistors. Each individual resistor R7, R8 and R9 can be shorted through control by Q12, Q13 and Q14 respectively. By selecting resistive elements R7, R8 and R9 as series resistors with

resistive element R6, the voltage V_{out} is changed. In a preferred embodiment of the present invention, the resistive element R5 equals 6380, the resistive element R6 equals 5880, the resistive element R7 equals 392, the resistive element R8 equals 787, and the resistive element R9 equals 1568. By setting the resistive elements R5-R9 to the above values and programming the transistors Q13, Q12, and Q14, the voltage V_{out} is generated to correspond to specific threshold temperatures. Specifically, Table 1 illustrates the threshold temperatures programmed in response to the input voltages Vp1, Vp2, and Vp3.

TABLE 1

Vp1	Vp2	Vp3	Threshold Temperature (Degrees C.)
0	0	0	70°
0	0	1	80°
0	1	0	90°
0	1	1	100°
1	0	0	110°
1	0	1	120°
1	1	0	130°
1	1	1	140°

Referring to FIG. 5, a current source including the bandgap reference circuit configured in accordance with the present invention is illustrated. The bandgap reference circuit comprises resistors R1, R2, and R3 and bipolar transistors Q1, Q2, Q3 and Q8. The operation of the bandgap reference circuit 120 is described above. However, the bandgap reference circuit of FIG. 5 also incorporates a gain stage with bipolar transistor Q8. In order to incorporate a gain stage, the collector of bipolar transistor Q3 is coupled to the base of bipolar transistor Q8. The constant bandgap reference voltage generated at the collector of bipolar transistor Q3 controls the base of bipolar transistor Q8 resulting in

a signal at the emitter of bipolar transistor Q8 containing a silicon bandgap voltage with increased current density. In addition to the bandgap reference circuit, FIG. 5 illustrates a constant current source 140 including a start-up circuit portion. The constant current source 140 comprises a bipolar transistor Q4, P-MOS transistors Q5, Q7 and Q15, and resistor R4. The constant current source 140 stabilizes operation of the thermal sensor of the present invention over a range of Vcc ranges.

In general, the constant current source 140 is derived from the generation of the constant bandgap reference voltage. In operation, the constant bandgap reference voltage, $V_{bandgap}$, is coupled to the base of bipolar transistor Q4. The constant bandgap reference voltage drives the bipolar transistor Q4 to generate a constant current flowing from the collector to the emitter of transistor Q4 and through the resistor R4. The P-MOS transistor Q5 is mirrored with P-MOS transistors Q7 and Q15. The constant current flowing through resistor R4 also flows through P-MOS transistor Q5 and is mirrored through P-MOS transistors Q7 and Q15. In a preferred embodiment, resistive element R4 equals 6020. The P-MOS transistor Q15 provides a constant current source for the programmable V_{be} circuit 110. Similarly, P-MOS transistor Q7 provides a constant current source to the bandgap reference circuit 120 through bipolar transistors Q3 and Q8.

The current source and bandgap reference voltage circuit illustrated in FIG. 5 also comprises a start-up circuit. The start-up circuit within the current source is required because the bandgap reference voltage controls the current source which, in turn, controls the bandgap reference voltage. Therefore, an equilibrium between the bandgap reference voltage and the current source circuit is required to ensure the proper operation of the

thermal sensor. The start-up circuit contains P-MOS transistors Q6, Q9 and Q10. The P-MOS transistor Q9 is configured such that the gate is coupled directly to the drain. In this configuration, the P-MOS transistor Q9 operates as a load resistor. In general, the start-up circuit generates a voltage for the bandgap reference voltage circuit during initial power-up of the thermal sensor. Specifically, during an initial power-up of the thermal sensor circuit, transistors Q5, Q7, Q10, and Q15 are biased such that no current flows through the respective devices. Also, during the initial power-up state, the P-MOS transistor Q9 is biased to conduct current thereby supplying a low voltage level to the gate of P-MOS transistor Q6. A low voltage level at the gate of P-MOS transistor Q6 biases the P-MOS transistor Q6 such that current flows from the Vcc to bipolar transistors Q3 and Q8. The P-MOS transistor Q6 biases the base of bipolar transistor Q8 allowing generation of the bandgap reference voltage.

An increase in the bandgap reference voltage driving the base of bipolar transistor Q4 causes current to flow from the emitter of Q4 through resistor R4. As the current density increases through transistors Q5 and Q10, the voltage at the gate of transistor Q6 also increases. The build up of charge at the gate of transistor Q6 is facilitated by a large resistance generated by the load transistor Q9. As the voltage at the gate of P-MOS transistor Q6 raises to the pinch-off threshold voltage of the device, the P-MOS transistor Q6 conducts no current such that current is no longer supplied to bipolar transistors Q3 and Q8. Because of the gain provided at the emitter of bipolar transistor Q8, current continues to increase in the bandgap reference voltage circuit until the collector of bipolar transistor Q3 begins to control the base of bipolar transistor Q8. At this point, the circuit has reached an equilibrium such that the constant bandgap reference voltage generated

supplies a constant voltage to the current source. Also shown in FIG. 5 is a disable P-MOS transistor Q21. The P-MOS transistor Q21 powers down, or disables, the thermal sensor circuit for testing. The P-MOS transistor Q21 is utilized only for disabling, and it is not required to generate the constant current source or the bandgap reference voltage. The P-MOS transistor Q15 isolates the collector of bipolar transistor Q11 on the programmable V_{be} circuit from the Vcc on the current source circuit.

Referring to FIG. 6, a sense amplifier for the thermal sensor configured in accordance with the present invention is illustrated. In a preferred embodiment of the present invention, a sense amplifier 160 contains three stages. The first stage and the second stage are identical. The third stage comprises a current buffer 600. The current buffer 600 is illustrated in FIG. 6 as a standard logic inverter. In general, the sense amplifier 160 operates as a comparator circuit. In operation, if the $V_{bandgap}$ is greater than the V_{out} voltage, then the output of sense amplifier 160 is a low logic level. Alternatively, if the V_{out} is greater than the $V_{bandgap}$ voltage, then the output of sense amplifier 160 is a high logic level. The second stage of sense amplifier 160 generates a voltage gain of signals on lines S1 and S1#. The first stage contains PMOS transistors Q16, Q17 and Q18, and NMOS transistors Q19 and Q20. The transistors Q19 and Q20 are constructed as a current mirror.

The voltage V_{out} is input to the gate of PMOS transistor Q16, and the voltage V_{gap} is input to the gate of PMOS transistor Q17. In operation, if the voltage V_{out} is greater than the $V_{bandgap}$, then PMOS transistor Q17 is biased to conduct more current than PMOS transistor Q16. Because a greater current density flows through PMOS transistor Q17 than PMOS transistor Q16, the voltage at line S1 rises and the voltage at line S1#

decreases. The source and gate of NMOS transistor Q19 are connected, and the source/gate connection is controlled by the voltage at S1#. Consequently, when the voltage at line S1# decreases, NMOS transistor Q19 is biased to reduce the current density flow. The voltage on line S1# is input to the gate of PMOS transistor Q18. As the voltage on line S1# decreases, the PMOS transistor Q18 is biased to conduct a greater current density. The increase in current density through transistor Q18 further amplifies the voltage difference between lines S1 and S1#. When the V_{be} voltage is less than the V_{gap} voltage, the first stage of the sense amplifier 160 operates in an analogous manner.

The second stage of sense amplifier 160 comprises PMOS transistors Q22, Q23 and Q24, and NMOS transistors Q25 and Q26. The operation of the second stage of the sense amplifier 160 is analogous to the operation of the first stage. In addition, hysteresis is provided for the sense amplifier 160 via a feedback path from the output of sense amplifier 160 to the programmable V_{be} circuit V_{out} input of sense amplifier 160. The hysteresis provides a more stable output signal from the sense amplifier 160 such that voltage variations on the inputs of the sense amplifier 160 after generation of a high output voltage level does not cause glitches in the output signal.

For the programmable thermal sensor of the present invention to operate well over process variations, the resistors are constructed to have a width larger than the minimum specification for the resistive value. All bipolar transistors in the programmable thermal sensor contain at least double width emitters. For the MOS transistors, long channel lengths are constructed. The long channel lengths of the MOS transistors help stabilize the programmable thermal sensor as well as provide noise immunity. For the bandgap reference circuit 120, the bipolar transistor Q2 is constructed to be ten times greater in

size than the bipolar transistor Q1. The large size differential between bipolar transistors Q1 and Q2 provides a stable bandgap voltage reference.

Referring to FIG. 7, a first embodiment of a microprocessor incorporating a programmable thermal sensor configured in accordance with the present invention is illustrated. A microprocessor 700 contains, in part, the programmable thermal sensor 100 and a processor unit 705. The processor unit 705 is intended to present a broad category of microprocessor circuits comprising a wide range of microprocessor functions. In general, the programmable thermal sensor 100 is programmed to detect a threshold temperature within the microprocessor 100. If the microprocessor 700 attains the pre-programmed threshold temperature, the programmable thermal sensor 100 generates an interrupt. As described above, the programmable thermal sensor 100 detects the pre-programmed threshold temperature based on the temperature of the integrated circuit at the programmable thermal sensor 100. The temperature across a microprocessor die can vary as much as 8° F. In a preferred embodiment of the present invention, the programmable thermal sensor 100 is located in the middle of the die of microprocessor 700 so as to provide the best thermal sensing. However, placement of the programmable thermal sensor in the middle of the die increases noise in the microprocessor. In an alternative embodiment, several thermal sensors are placed across the microprocessor die. In this configuration, each thermal sensor provides an interrupt when attaining the threshold temperature, and an average temperature is calculated based on the several thermal sensors.

In addition to the programmable thermal sensor 100 and processor unit 705, a microprocessor 700 contains an internal register 735, a read only memory (ROM) 730,

and a phase lock loop (PLL) circuit 720. External to the microprocessor 700 is an external clock 710. The external clock 710 provides a clock signal to the PLL circuit 720. The PLL circuit 720 permits fine tuning and variable frequency adjustment of the input clock signal. Specifically, the PLL circuit 720 receives a value, and increases or decreases the frequency based on the value received. The PLL circuit 720 is intended to represent a broad category of frequency adjustment circuits, which are well known in the art and will not be described further. The output of the PLL circuit 720 is the microprocessor system clock, and is input to the processor unit 705.

The programmable thermal sensor 100 is coupled to the ROM 730 and internal register 735. The ROM 730 contains a microprogram consisting of a plurality of microcode instructions. The operation of the microprogram within the microprocessor 700 is described more fully below. In general, the microprogram 740 writes values representing the threshold temperature in the internal register 735. The internal register 735 stores the threshold temperature values and is coupled to the programmable V_{be} circuit 110. For example, in a preferred embodiment of the present invention, the Vp1, Vp2 and Vp3 voltage values stored in the internal register 735 are used to program the programmable V_{be} circuit 110 in the manner as described above. However, the present invention is not limited to three input voltage values in that any number of values may be stored in the internal register 735 to program any number of threshold temperatures. When the microprocessor 700 attains the threshold temperature, the programmable threshold sensor generates a comparator signal via sense amplifier 160 as described above. The comparison signal is labeled as "interrupt" on FIG. 7. The interrupt is input to the ROM 730 and the processor unit 705.

In response to the interrupt, the microprogram 740 generates new values representing a new threshold temperature. The microprogram writes the new values to the internal register 735. For example, if the programmable thermal sensor generates an interrupt based on a threshold temperature of 100°° F, then the microprogram may write values to the internal register 735 to represent a threshold temperature of 110 F. In the first embodiment, the processor unit 705 receives the interrupt signal as a standard hardware interrupt input. In response to the interrupt, the processor unit 705 generates a clock control value for the PLL circuit 720. The clock signal value reduces the microprocessor system clock frequency.

If the interrupt is again generated in response to the microprocessor 700 attaining the new threshold temperature value, the microprogram 740 writes a new temperature threshold value to the internal register 735, and the processor unit 705 further reduces the microprocessor system clock frequency. In addition, the processor unit 705 may set a standard timer circuit such that if a pre-determined amount of time elapses, then the processor unit 705 increases the clock frequency. Increasing the clock frequency permits the processor unit 705 to increase performance when the temperature of the microprocessor has decreased. In addition, to detect further decreases in the microprocessor temperature, the microprogram 740 may lower the threshold temperature and the processor unit may further increase the clock frequency. Therefore, the programmable thermal sensor of the present invention is utilized to control the temperature by increasing and decreasing the microprocessor clock frequency.

Referring to FIG. 8, a flow diagram for a method of controlling the programmable thermal sensor configured in accordance with the present invention is

illustrated. The method illustrated in the flow chart of FIG. 8 may be a microprogram such as microprogram 740 stored in ROM 730. Upon initialization of the microprocessor, a first threshold temperature is programmed into the programmable thermal sensor as shown in step 800. Although the present invention is described in conjunction with a microprocessor integrated circuit, one skilled in the art will appreciate that the thermal sensor of the present invention may be incorporated into any integrated circuit. The temperature of the integrated circuit is sensed as shown in step 810. The sensing of the integrated circuit may be performed by the programmable thermal sensor 110 of the present invention. The integrated circuit sensor determines whether the temperature of the integrated circuit equals the first threshold temperature. If the integrated circuit temperature is equal to or greater than the threshold temperature, then the threshold temperature is compared to a critical temperature as shown in step 830.

The critical temperature is defined as the maximum temperature that the integrated circuit may attain before the integrated circuit is physically damaged. If the threshold temperature is equal to the critical temperature, then the integrated circuit is shut down as shown in step 860. Alternatively, if the threshold temperature is less than the critical temperature, then steps are taken to reduce the temperature in the integrated circuit as shown in step 840. For example, in a microprocessor integrated circuit, the microprocessor system clock frequency is reduced. In addition to reducing the system clock frequency, a message to a system user reporting the temperature of the integrated circuit is generated. By informing the user with the temperature information, the user may take steps external to the integrated circuit to facilitate cooling. Next, a new threshold temperature is programmed in the thermal sensor as shown in step 850. The

process continues wherein the thermal sensor senses the integrated circuit temperature to detect if the integrated circuit temperature reaches the new threshold temperature, and based on the threshold temperature set, either shuts down the power to the integrated circuit or executes steps to reduce the temperature.

Referring to FIG. 9, a block diagram of a programmable thermal sensor system configured in accordance with a second embodiment of the present invention is illustrated. A microprocessor 900 comprises, in part, a programmable thermal sensor 110 and a processor unit 905. The programmable thermal sensor 110 is configured as described above. The programmable thermal sensor 110 is connected to a ROM 910 and an internal register 920. The programmable thermal sensor 110 is also coupled to external sensor logic 940. The external sensor logic 940 is coupled to a counter 950 and an active cooling device 955. An external clock 945 is input to a counter 950, and the output of the counter 950 is input to a clock circuit 930. The clock circuit 930 buffers the input clock frequency to generate the microprocessor clock for the processor unit 905. In operation, a microprogram 915, stored in ROM 910, sets the internal register 920 to an initial threshold temperature value. If the temperature of the microprocessor 900 rises to the threshold temperature, an interrupt signal is generated to the external sensor logic 940.

Upon receipt of the interrupt to the external sensor logic 940, the external sensor logic 940 programs a value to the counter 950, and activates the active cooling device 955. The active cooling device 955 may comprise a fan or other heat dissipating device. To activate the active cooling device 955, the external sensor logic 940 generates a signal to turn on the active cooling device 955 by any number of well known methods. The

counter 950 is configured as a frequency divider such that a clock frequency, from the external clock 945, is input. The counter 950 generates a new clock frequency based on the counter value. The programming of a counter, such as counter 950, for use as a frequency divider is well known in the art and will not be described further. As one skilled in the art will recognize, the amount in which the clock frequency may be reduced is a function of the counter selected. The slower clock frequency is input to the clock circuit 930. The clock circuit 930 may perform a variety of functions such as buffering, clock distribution, and phase tuning. The system clock comprises a reduced frequency to facilitate the cooling of the device. In addition to triggering the external sensor logic 940, the programmable thermal sensor also interrupts the microprogram 915. Upon receiving the interrupt, the microprogram 915 programs the internal register 920 to sense a new threshold temperature. If the microprocessor 900 heats up to the new threshold temperature, the external sensor logic 940 is again triggered, and the system clock frequency is further reduced. The configuration illustrated in FIG. 9 provides closed loop control of the microprocessor system clock frequency, thereby automatically reducing the temperature when overheating occurs.

Referring to FIG. 10, a block diagram of a fail safe thermal sensor configured in accordance with the present invention is illustrated. A fail safe thermal sensor 1010 is incorporated into a microprocessor 1000. Although the fail safe thermal sensor 1010 is incorporated into the microprocessor 1000, one skilled in the art will appreciate the fail safe thermal sensor may be incorporated into any integrated circuit. The fail safe thermal sensor 1010 contains a V_{be} circuit 1012, a bandgap voltage reference circuit 120, a current source 140, and a sense amplifier 160. The bandgap voltage reference circuit

120, the current source 140 and the sense amplifier 160 operate in accordance with the respective circuits described above. The V_{be} reference circuit 1012 is equivalent to the programmable V_{be} circuit 110, except that the resistive value ratio is fixed. In the V_{be} circuit 1012, the output V_{be} voltage is fixed based on resistive values R5, R6, R7, R8 and R9. In a preferred embodiment of the present invention, the resistive values R5, R6, R7, R8 and R9 are fixed to the critical temperature. Consequently, the fail safe thermal circuit 1010 generates an interrupt when the temperature of the microprocessor 1000 attains the pre-programmed fixed critical temperature.

The output of the fail safe thermal sensor 1010 is connected to stop clock logic 1015. The stop clock logic 1015 is coupled to the microprocessor clock circuit 1020. Upon receipt of the interrupt of the fail safe thermal sensor 1010, the stop clock logic 1015 halts operation of the microprocessor 1000 by inhibiting the microprocessor clock. In addition, the stop clock logic 1015 ensures that the microprocessor 1000 finishes a system cycle completely. The stop clock logic 1015 therefore protects loss of data when an interrupt is generated during a microprocessor clock cycle. A microprocessor clock circuit 1012 may comprise a simple clock oscillator or a more complex and controllable clock generator. The fail safe thermal sensor 1010 prohibits the microprocessor 1000 from attaining a critical temperature, thereby protecting the device without software control.

Referring to FIG. 11, a computer system incorporating a microprocessor comprising thermal sensing configured in accordance with the present invention is illustrated. A computer system 1100 contains a central processing unit (CPU) 1105 incorporating the programmable thermal sensor 100 and the fail safe thermal sensor

1010. In a preferred embodiment, the CPU comprises a compatible Intel microprocessor architecture, manufactured by Intel Corporation, the assignee of the present invention. The computer system 1100 also contains memory 1110 and an I/O interface 1120. The I/O interface 1120 is coupled to an output display 1130 and input devices 1140 and 1145. In addition, I/O interface 1120 is coupled to a mass memory device 1160. The CPU 1105, memory 1110, I/O interface 1120, output device 1130, and input devices 1140 and 1145 are those components typically found in a computer system, and, in fact, the computer system 1100 is intended to represent a broad category of data processing devices. The memory 1110 stores software for operation of the computer system 1100. Specifically, memory 1110 stores, in part, an operating system and an interrupt handler routine for operation in conjunction with the thermal sensor.

Upon generation of an interrupt in the programmable thermal sensor 100 or the fail safe thermal sensor 1010, the interrupt handler routine 1165 is executed. The calling of an interrupt handler routine upon generation of a hardware interrupt in a microprocessor is well-known in the art and will not be described further. In general, the interrupt handler routine 1165 generates a message to the output display 1130. The message informs the user of the computer system 1100 that the microprocessor 1105 has attained the threshold temperature. In response, a user may alter external environmental conditions to facilitate cooling of the CPU 1105. As described above, the CPU 1105 sets a new threshold temperature for the programmable thermal sensor. If the CPU 1105 temperature rises to the new threshold temperature, another interrupt is generated. Again, the interrupt handler routine 1165 is called to generate a message to the user on output display 1130. If the temperature reaches a critical temperature for which the fail safe

thermal sensor is programmed, then the fail safe thermal sensor generates an interrupt to shut down the CPU 1105.

Although the present invention has been described in terms of a preferred embodiment, it will be appreciated that various modifications and alterations might be made by those skilled in the art without departing from the spirit and scope of the invention. The invention should therefore be measured in terms of the claims which follow.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a fail safe sensor;

halt logic to halt operation of the integrated circuit in response to the fail safe sensor indicating that a threshold temperature has been exceeded.

2. The integrated circuit of Claim 1 wherein the threshold temperature is a predetermined fixed critical temperature.

3. The integrated circuit of Claim 1 wherein the halt logic is to inhibit operation of the integrated circuit by stopping a clock for the integrated circuit.

4. The integrated circuit of Claim 1 wherein the halt logic protects the integrated circuit without software control.

5. The integrated circuit of Claim 1 comprising:

a plurality of thermal sensors placed across the integrated circuit;

an averaging mechanism in communcation with the fail-safe sensor to calculate an average temperature from the plurality of thermal sensors.

6. The integrated circuit of Claim 1 further comprising clock adjustment logic in communication with the fail-safe sensor to control temperature of the integrated circuit by increasing and decreasing a clock frequency of the integrated circuit.

7. The integrated circuit of Claim 1 further comprising clock adjustment logic in communication with the fail-safe sensor to execute instructions to provide closed loop control of the integrated circuit clock frequency, thereby automatically reducing the temperature when overheating occurs.

8. The integrated sensor of Claim 1 further comprising clock adjustment logic in communication with the fail-safe sensor to decrease a clock frequency of the integrated circuit in response to the fail-safe sensor indicating that a threshold temperature value has been exceeded.

9. The integrated circuit of Claim 1 further comprising threshold adjustment logic in communication with the fail-safe sensor to increase the threshold temperature value to a new threshold temperature value in response to the fail-safe sensor indicating that the threshold temperature value has been exceeded.

10. The integrated circuit of Claim 8 wherein the threshold adjustment logic is further to lower the new threshold temperature to detect decreases in temperature.

11. The integrated circuit of Claim 1 further comprising an interrupt handler to display information regarding a temperature sensed by the fail-safe sensor to a user of the integrated circuit.

12. A method comprising:

sensing a temperature of an integrated circuit;

halting operation of the integrated circuit in response to a threshold temperature being exceeded.

13. The method of Claim 12 wherein the threshold temperature is a predetermined fixed critical temperature.

14. The method of Claim 12 wherein halting operation comprises inhibiting operation of the integrated circuit by stopping a clock for the integrated circuit.

15. The method of Claim 12 wherein halting operation comprises halting operation of the integrated circuit without software control.

16. The method of Claim 12 further comprising controlling the temperature of the integrated circuit by increasing and decreasing a clock frequency of the integrated circuit in response to the sensed temperature.

17. The method of Claim 12 further comprising executing instructions to provide closed loop control of the integrated circuit clock frequency in response to the sensed temperature.

18. The method of Claim 12 further comprising decreasing a clock frequency of the integrated circuit in response to the sensed temperature indicating that a threshold temperature value has been exceeded.

19. The integrated circuit of Claim 12 further comprising displaying information regarding a sensed temperature to a user of the integrated circuit.

ABSTRACT

A fail-safe thermal sensor is implemented in an integrated circuit such as a microprocessor. The fail-safe thermal sensor monitors the temperature of the integrated circuit and halt logic halts operation of the integrated circuit in response to the fail-safe thermal sensor indicating that a threshold temperature has been exceeded. The threshold temperature may be a predetermined fixed critical temperature. The halt logic may inhibit operation of the integrated circuit by stopping a clock for the integrated circuit.

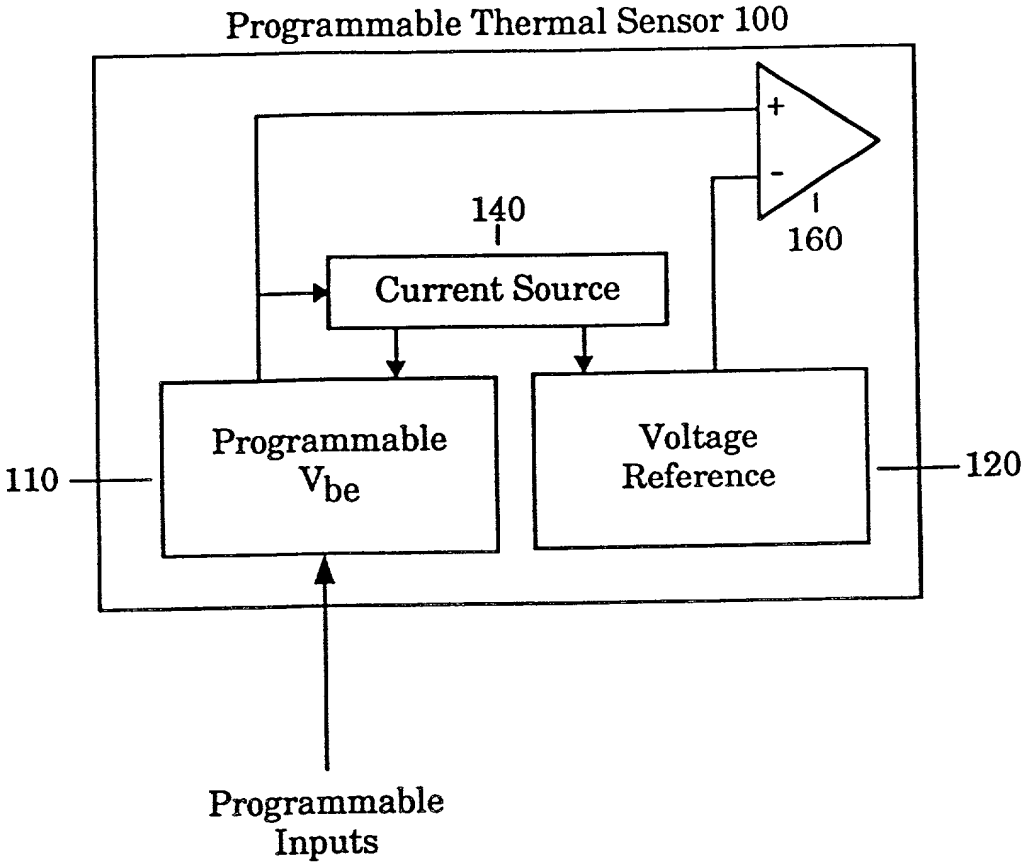
Programmable Thermal Sensor 100
+
-
140
160
Current Source
Programmable
V_{be}
Voltage
Reference
110
120
Programmable
Inputs

Figure 1

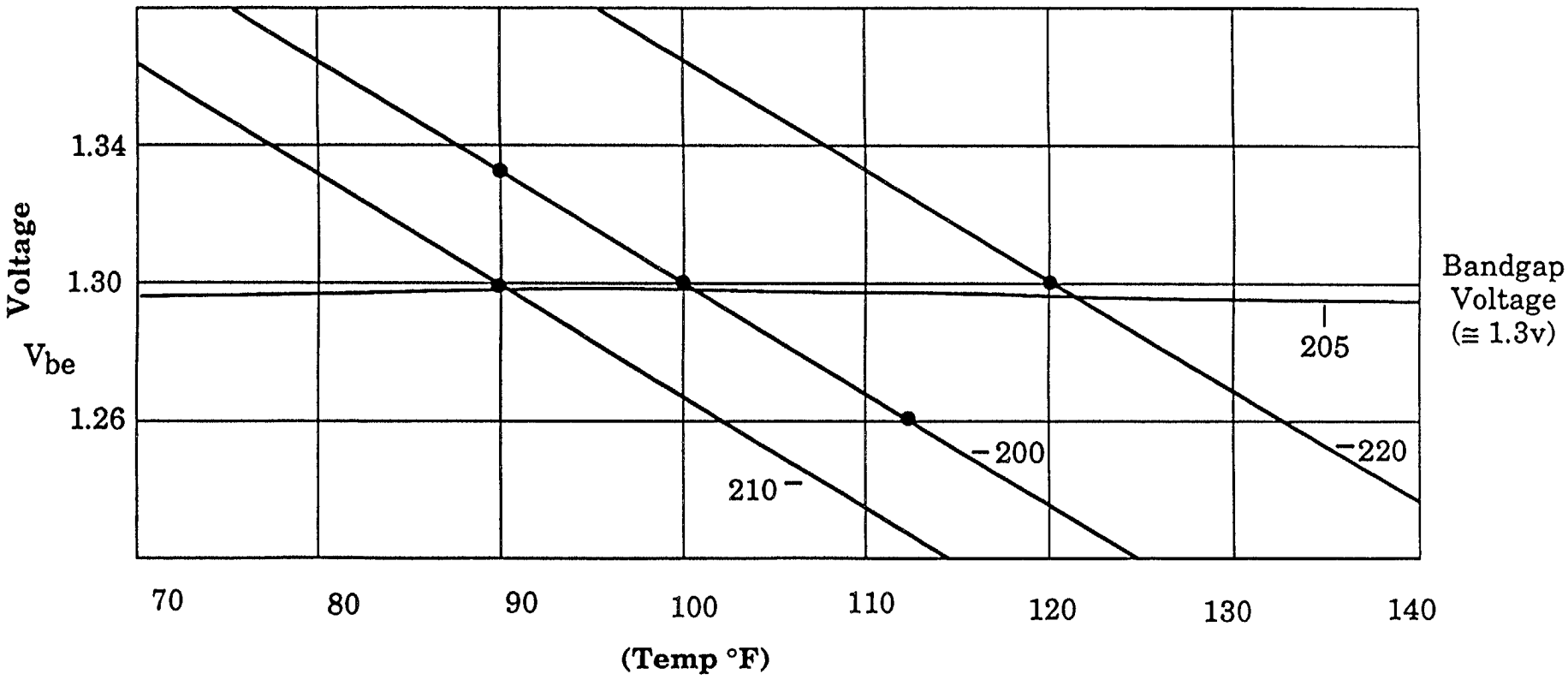

Figure 2

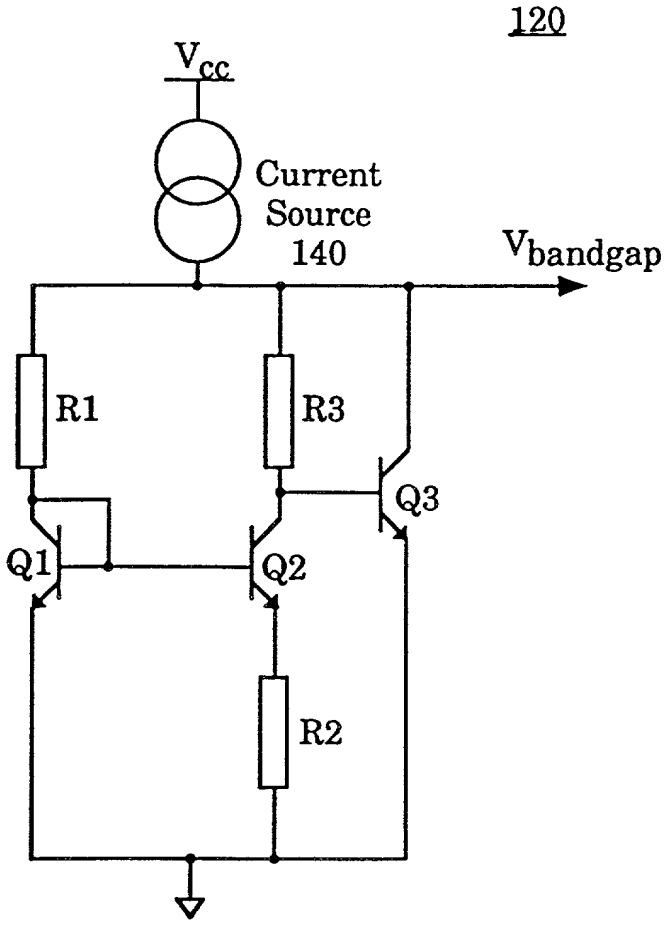

Figure 3

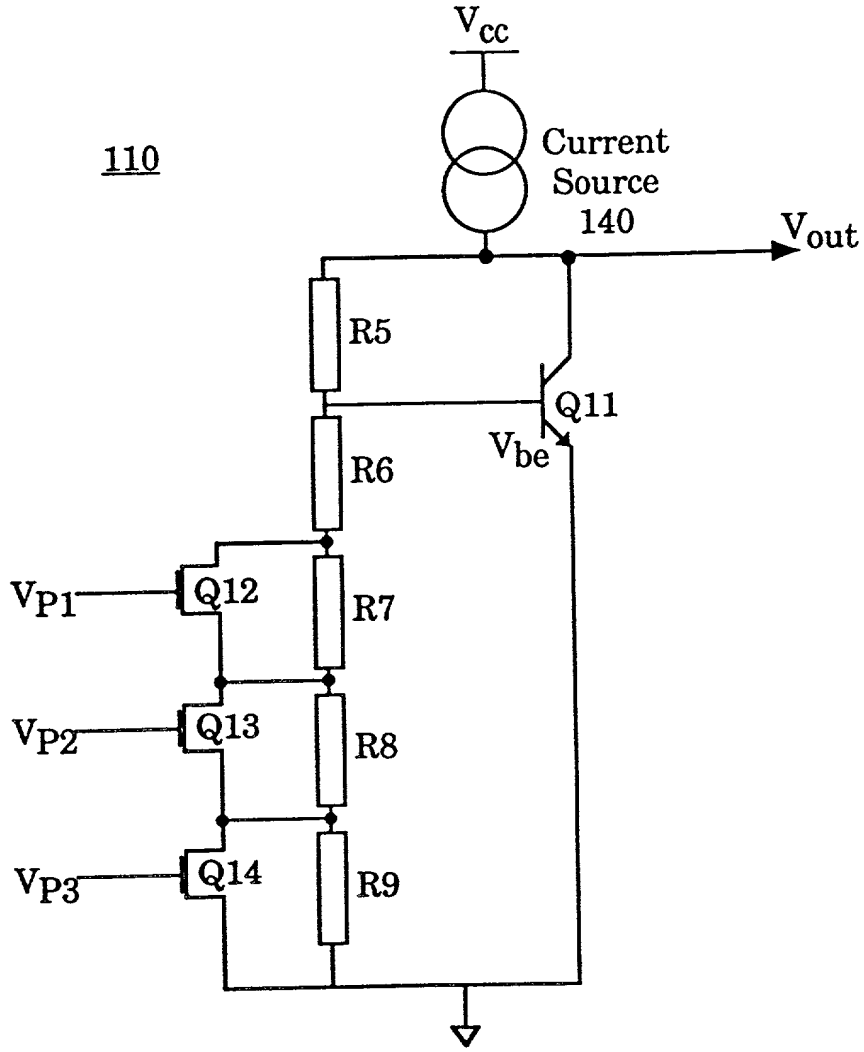
110
Vcc
Current
Source
140
Vout
R5
Q11
Vbe
R6
VP1
Q12
R7
VP2
Q13
R8
VP3
Q14
R9

Figure 4

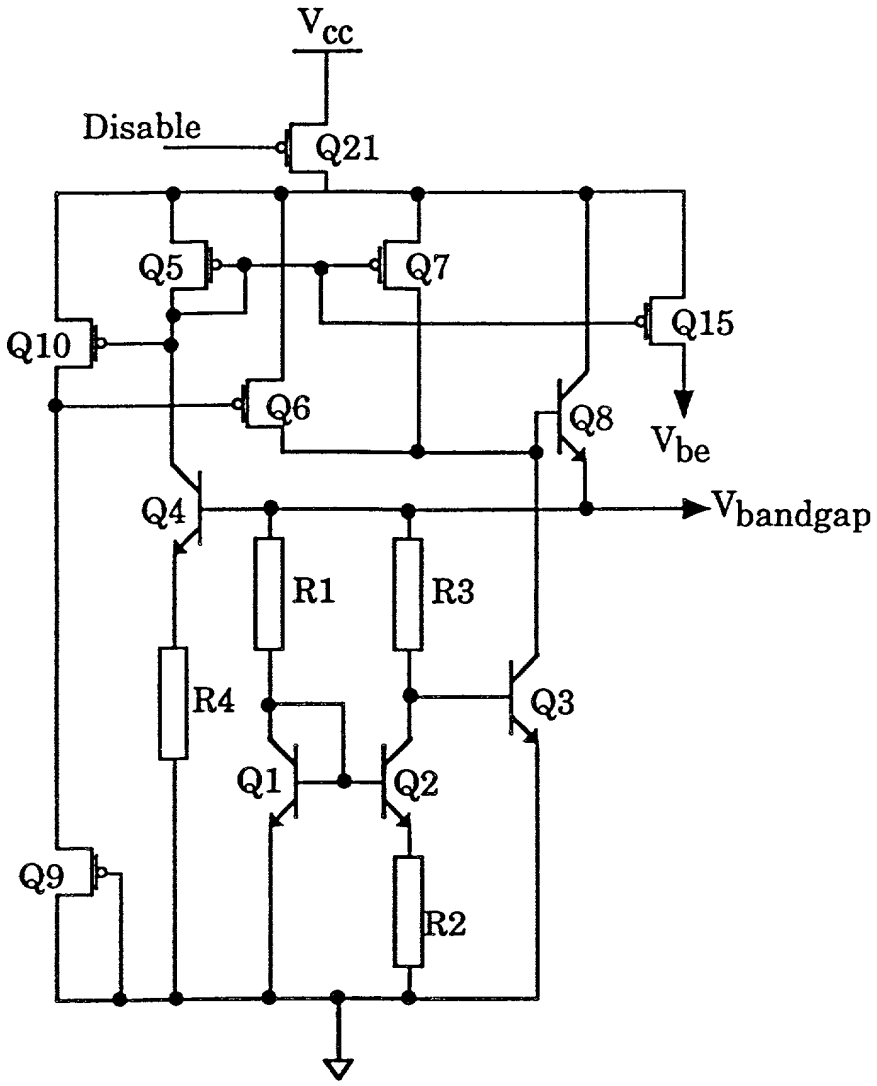
Vcc
Disable
Q21
Q5
Q7
Q15
Q10
Q6
Q8
Vbe
Q4
Vbandgap
R1
R3
R4
Q3
Q1
Q2
Q9
R2

Figure 5

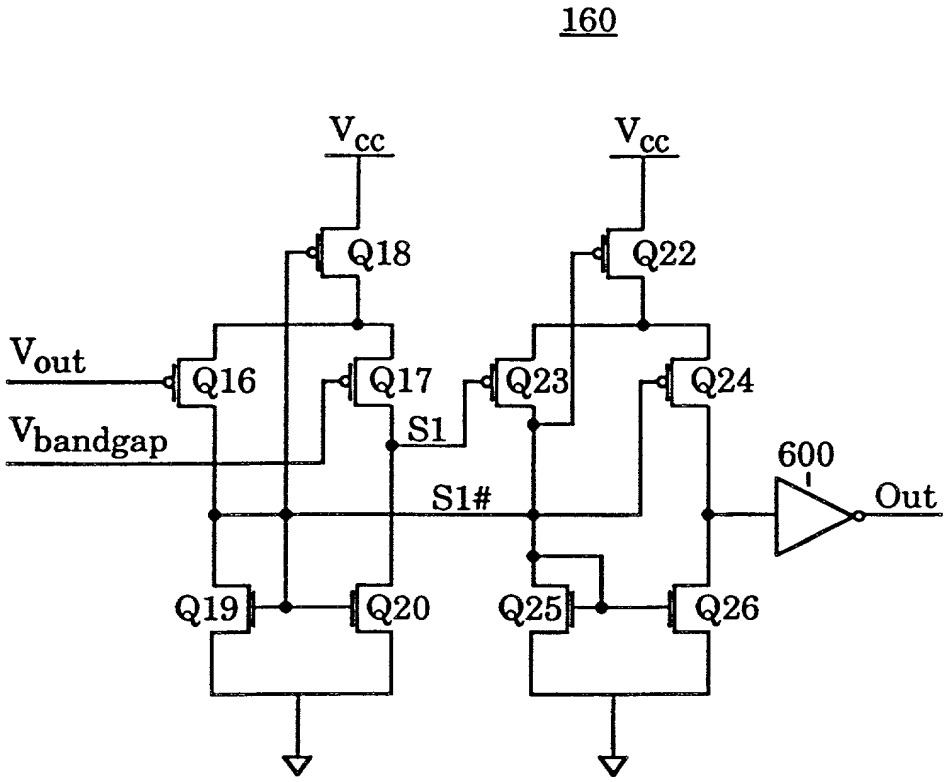
160
V_{cc}
V_{cc}
Q18
Q22
V_{out}
Q16
Q17
Q23
Q24
$V_{bandgap}$
S1
S1#
600
Out
Q19
Q20
Q25
Q26

Figure 6

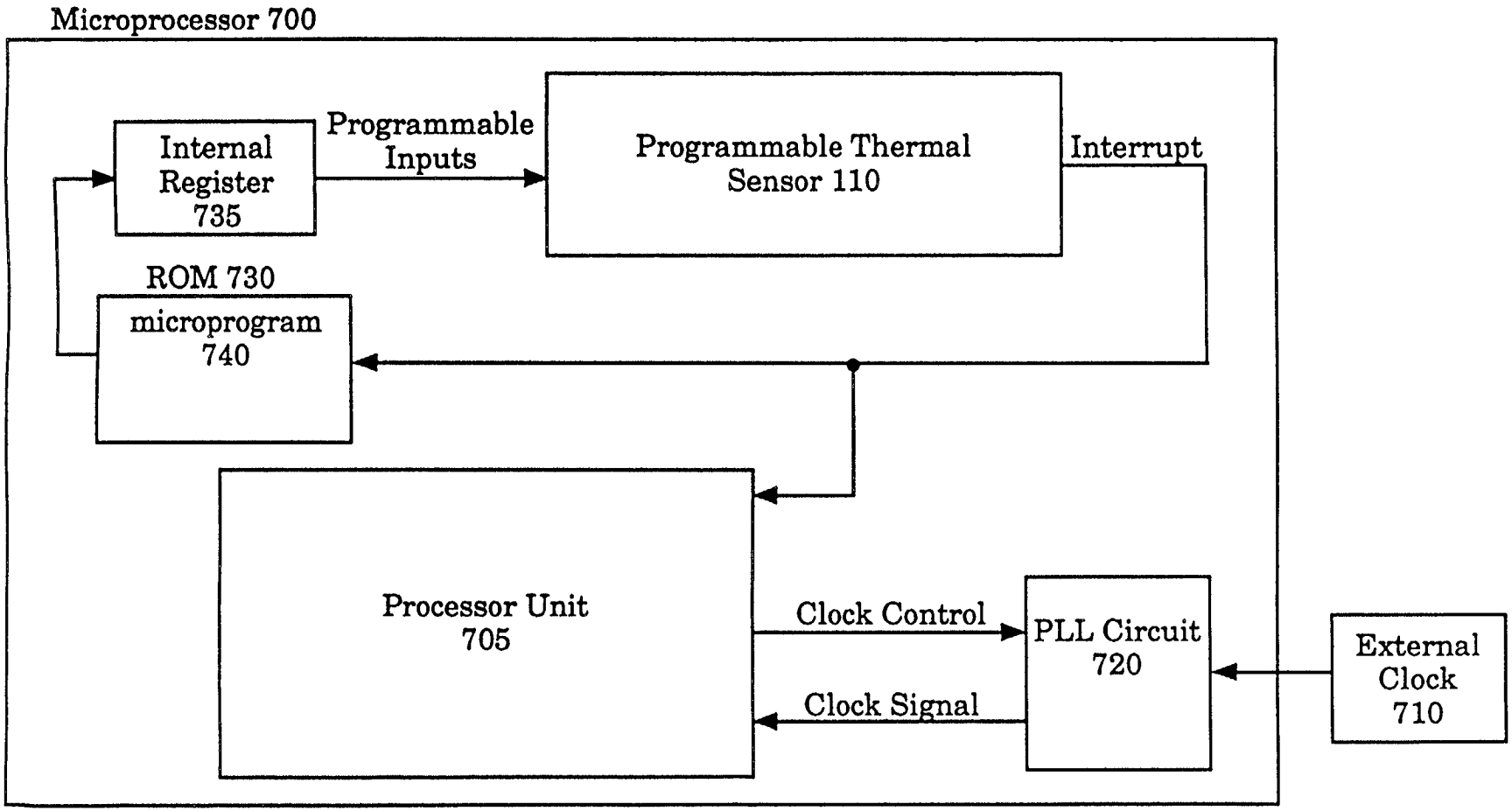
Microprocessor 700
Internal Register 735
Programmable Inputs
Programmable Thermal Sensor 110
Interrupt
ROM 730
microprogram 740
Processor Unit 705
Clock Control
Clock Signal
PLL Circuit 720
External Clock 710

Figure 7

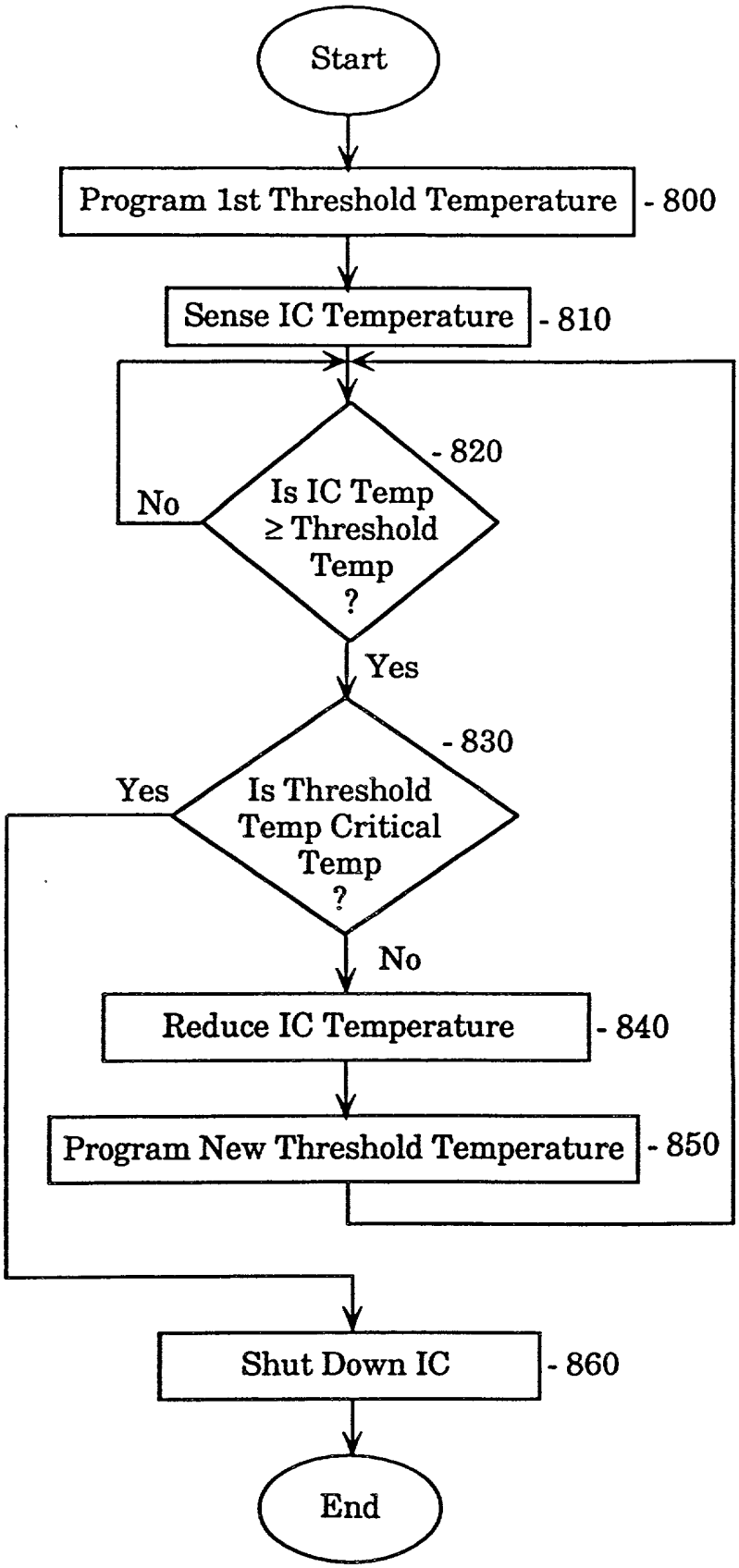
Start
Program 1st Threshold Temperature
- 800
Sense IC Temperature
- 810
- 820
No
Is IC Temp ≥ Threshold Temp ?
Yes
- 830
Yes
Is Threshold Temp Critical Temp ?
No
Reduce IC Temperature
- 840
Program New Threshold Temperature
- 850
Shut Down IC
- 860
End

Figure 8

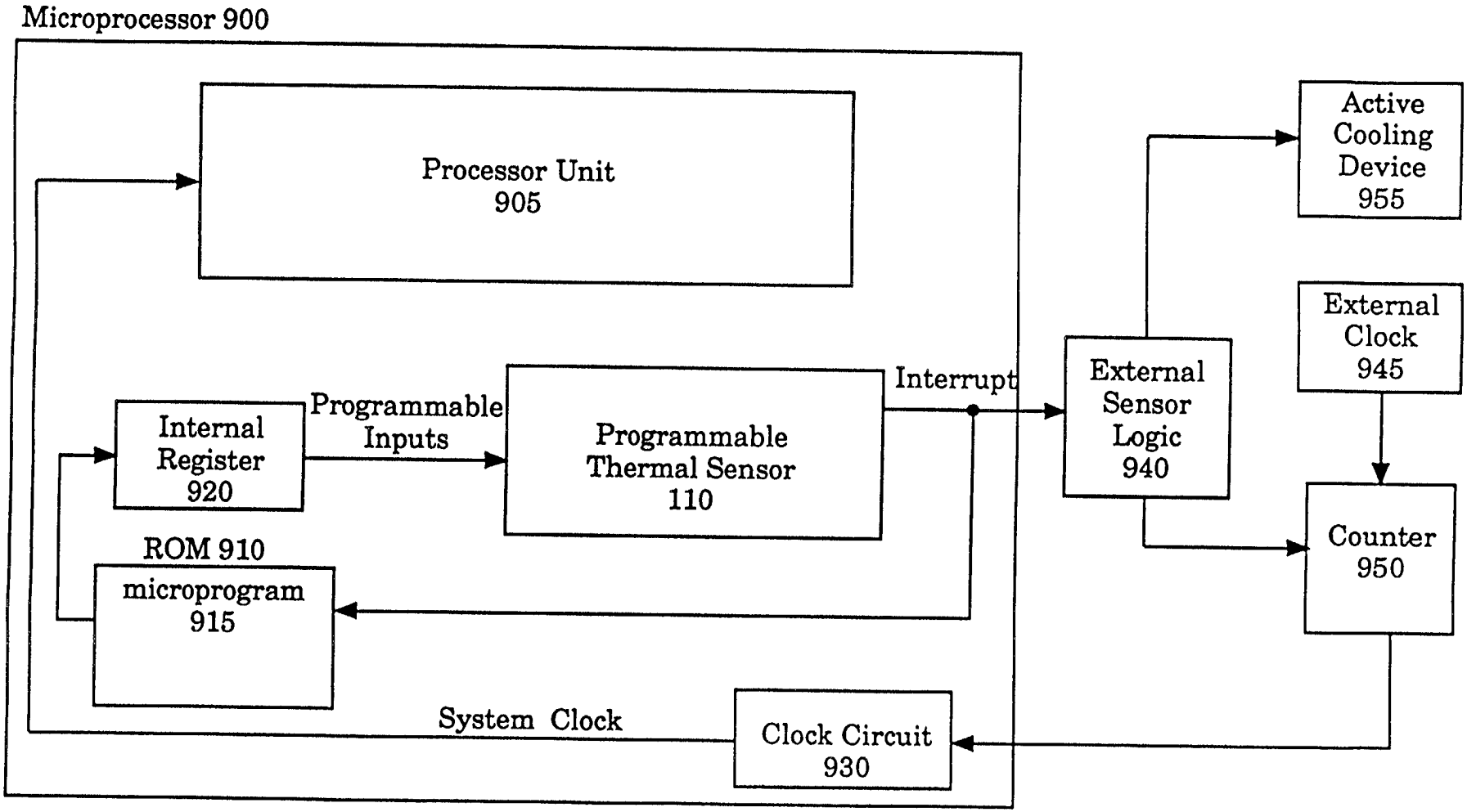
Microprocessor 900
Processor Unit
905
Internal
Register
920
Programmable
Inputs
Programmable
Thermal Sensor
110
Interrupt
ROM 910
microprogram
915
System Clock
Clock Circuit
930
External
Sensor
Logic
940
Active
Cooling
Device
955
External
Clock
945
Counter
950

Figure 9

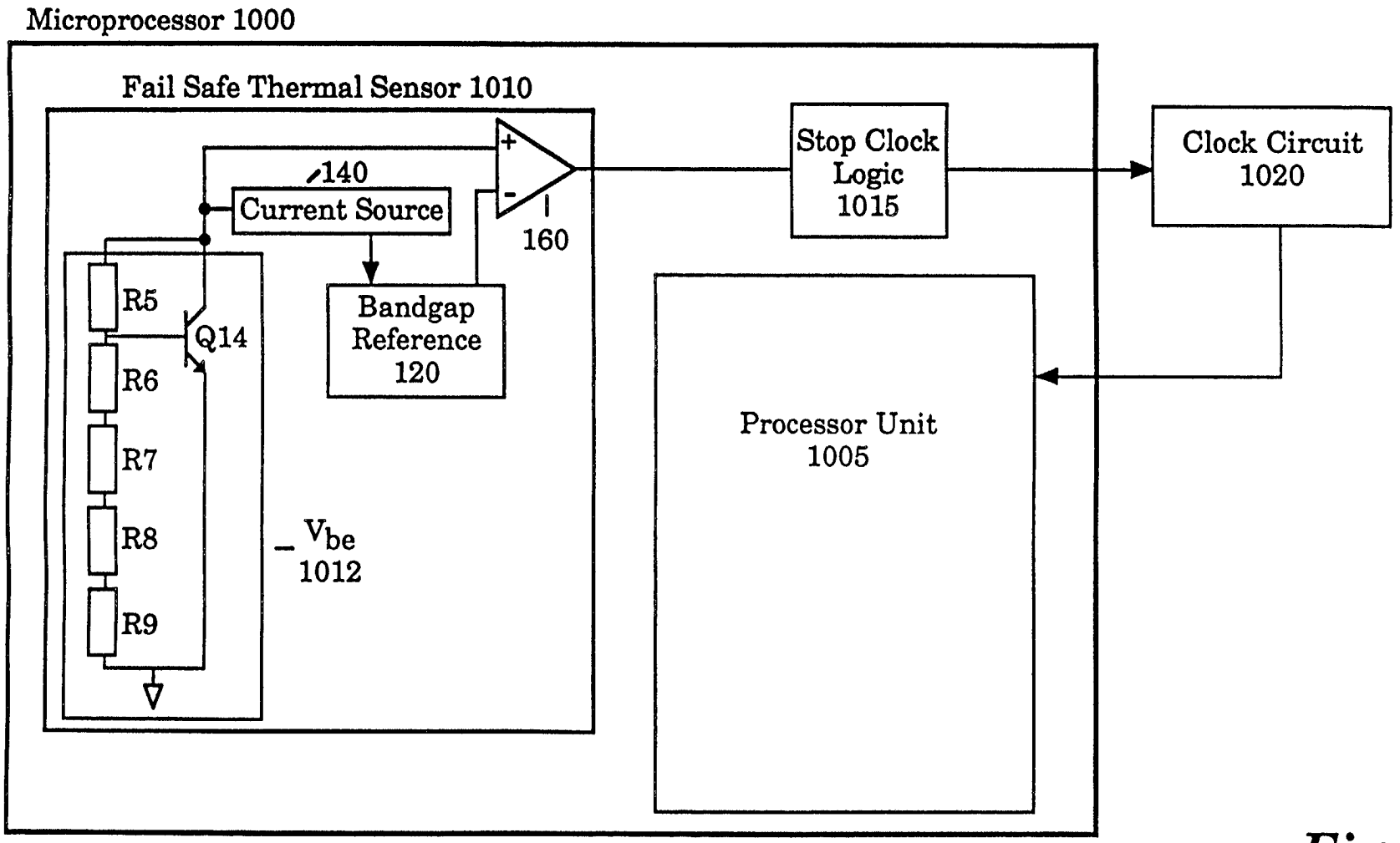
Microprocessor 1000
Fail Safe Thermal Sensor 1010
140
Current Source
160
Bandgap Reference 120
R5
Q14
R6
R7
R8
R9
Vbe 1012
Stop Clock Logic 1015
Clock Circuit 1020
Processor Unit 1005

Figure 10

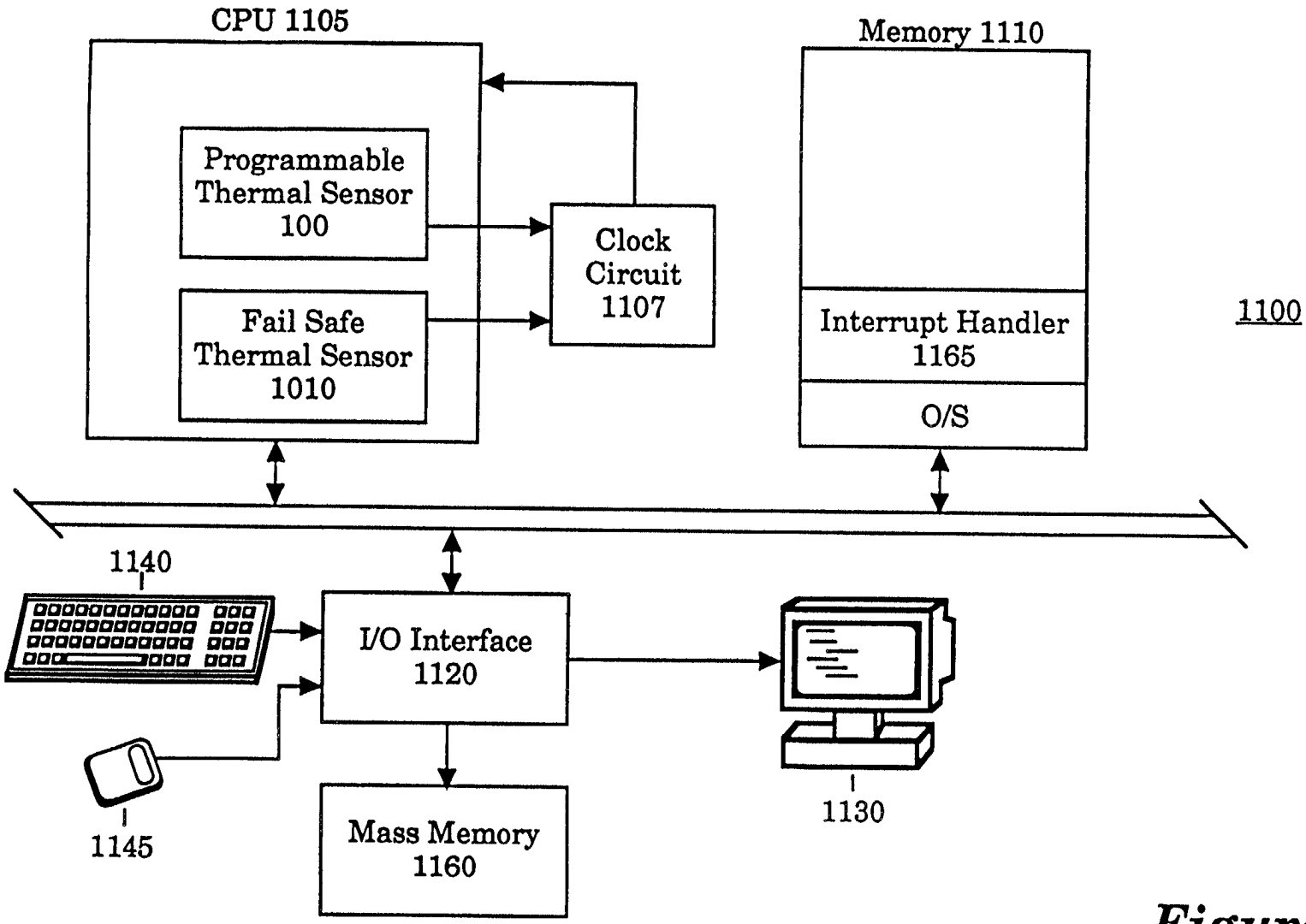

Figure 11

Attorney's Docket No.: 042390.P1674D4 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
Fail-Safe Thermal Sensor Apparatus and Method

the specification of which

_X_ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Gordon R. Lindeen III **(Name of Attorney or Agent)**, **BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** Gordon R. Lindeen III **(Name of Attorney or Agent)**, **(303) 740-1980.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Jack D. Pippin

Inventor's Signature Jack D. Pippin Date Nov 1, 2000

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Full Name of Second/Joint Inventor _____

Inventor's Signature _____ Date _____

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Full Name of Third/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.